IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Atsushi Nishizawa

Serial No.: 09/751,979

Filed: 12/29/2000

MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING SIMULTANEOUS FORMATION OF VIA HOLE REACHING METAL WIRING AND CONCAVE GROOVE IN INTERLAYER FILM AND SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURED WITH THE MANUFACTURING METHOD

ART UNIT: 1763

SUBMISSION OF REPLACEMENT SHEETS FOR FORMAL DRAWINGS

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

SIR:

Enclosed please find the replacement sheet for figures 1 through 7c in the above referenced application.

Any fee due with this paper, not fully covered by an enclosed check, may be charged to Deposit Acct. No. 50-1290.

Respectfully submitted,

Michael I. Markowitz
Reg. No. 30,659

Customer Number: 026304
Telephone: (212) 940-8800
Fax: (212) 940-8776
Date: August 18, 2004
Docket No.: NECW 18.159 (100806-17346)
Ach: fdraw

Filed Express Mail
(Receipt No. EL 790328024 US
on 08/18/04
pursuant to 37 C.F.R. 1.10.
by